

74LVC1G66

Bilateral switch

Rev. 12 — 12 January 2022

Product data sheet

1. General description

The 74LVC1G66 is a single-pole, single-throw analog switch with two input/output terminals (nY and nZ) and a digital enable input (nE). When nE is LOW, the analog switch is turned off. Control inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at control inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
 - 7.5 Ω (typical) at $V_{CC} = 2.7$ V
 - 6.5 Ω (typical) at $V_{CC} = 3.3$ V
 - 6 Ω (typical) at $V_{CC} = 5$ V
- Switch current capability of 32 mA
- High noise immunity
- CMOS low power consumption
- TTL interface compatibility at 3.3 V
- Overvoltage tolerant control inputs to 5.5 V
- Latch-up performance meets requirements of JESD78 Class I
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G66GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G66GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G66GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G66GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G66GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

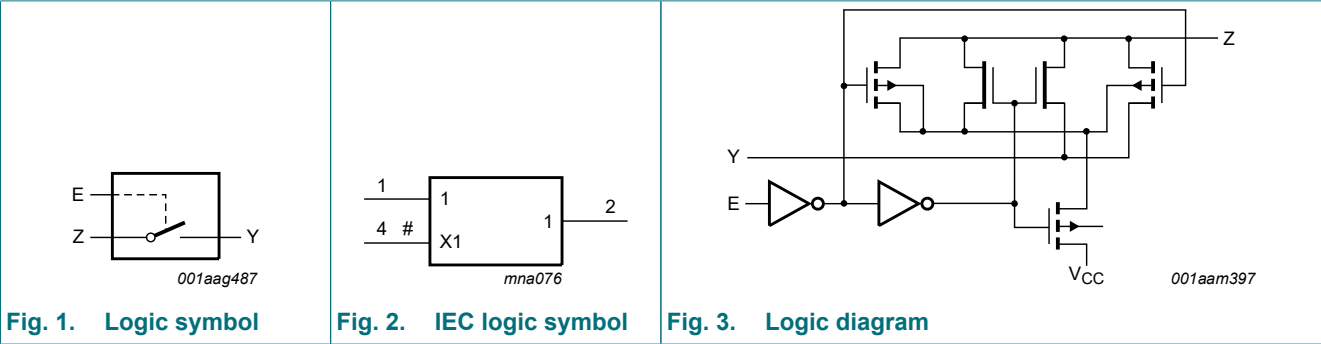
4. Marking

Table 2. Marking

Type number	Marking code [1]
74LVC1G66GW	VL
74LVC1G66GV	V66
74LVC1G66GM	VL
74LVC1G66GN	VL
74LVC1G66GS	VL

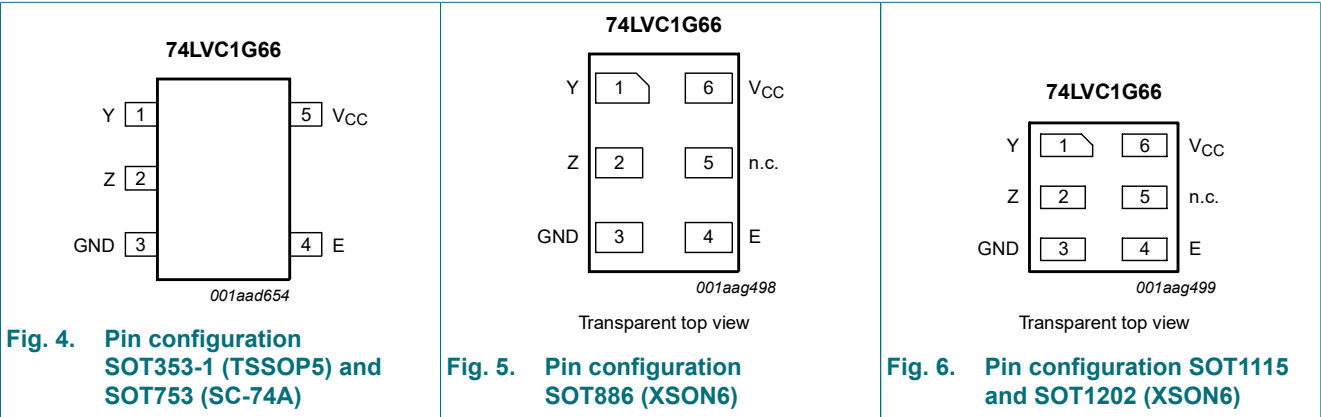
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT353-1, SOT753	SOT886, SOT1115 and SOT1202	
Y	1	1	independent input or output
Z	2	2	independent output or input
GND	3	3	ground (0 V)
E	4	4	enable input (active HIGH)
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input E	Switch
L	OFF-state
H	ON-state

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
V _I	input voltage	[1]	-0.5	+6.5	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±50	mA
V _{SW}	switch voltage	enable and disable mode [2]	-0.5	V _{CC} + 0.5	V
I _{SW}	switch current	V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	250	mW

- [1] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.
- [3] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.
For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_{SW}	switch voltage	[1]	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$ [2]	-	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$ [2]	-	-	10	ns/V

[1] To avoid sinking GND current from terminal Z when switch current flows in terminal Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Y. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
I_I	input leakage current	pin E; $V_I = 5.5\text{ V or GND}$; $V_{CC} = 0\text{ V to }5.5\text{ V}$ [2]	-	± 0.1	± 1	-	± 1	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5\text{ V}$; see Fig. 7 [2]	-	± 0.1	± 0.2	-	± 0.5	μA
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5\text{ V}$; see Fig. 8 [2]	-	± 0.1	± 1	-	± 2	μA
I_{CC}	supply current	$V_I = 5.5\text{ V or GND}$; $V_{SW} = \text{GND or }V_{CC}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$ [2]	-	0.1	4	-	4	μA
ΔI_{CC}	additional supply current	pin E; $V_I = V_{CC} - 0.6\text{ V}$; $V_{SW} = \text{GND or }V_{CC}$; $V_{CC} = 5.5\text{ V}$ [2]	-	5	500	-	500	μA
C_I	input capacitance		-	2.0	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	6.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	11	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25\text{ °C}$.

[2] These typical values are measured at $V_{CC} = 3.3\text{ V}$.

10.1. Test circuits

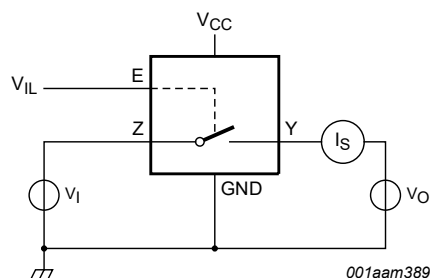
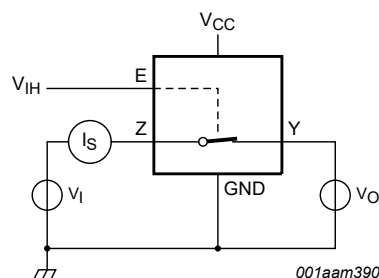

$$V_I = V_{CC} \text{ or GND and } V_O = \text{GND or } V_{CC}.$$

Fig. 7. Test circuit for measuring OFF-state leakage current



$V_I = V_{CC}$ or GND and $V_O =$ open circuit.

Fig. 8. Test circuit for measuring ON-state leakage current

10.2. ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 9; for graphs see Fig. 10 to Fig. 15.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	V _I = GND to V _{CC}						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	34.0	130	-	195	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	12.0	30	-	45	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	10.4	25	-	38	Ω
		I _{SW} = 24 mA; V _{CC} = 3.0 V to 3.6 V	-	7.8	20	-	30	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	6.2	15	-	23	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = GND						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	8.2	18	-	27	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.1	16	-	24	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	6.9	14	-	21	Ω
		I _{SW} = 24 mA; V _{CC} = 3.0 V to 3.6 V	-	6.5	12	-	18	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	5.8	10	-	15	Ω
		V _I = V _{CC}						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	10.4	30	-	45	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.6	20	-	30	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	7.0	18	-	27	Ω
		I _{SW} = 24 mA; V _{CC} = 3.0 V to 3.6 V	-	6.1	15	-	23	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	4.9	10	-	15	Ω

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} [2]						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	3.5	-	-	-	Ω
		I _{SW} = 24 mA; V _{CC} = 3.0 V to 3.6 V	-	2.0	-	-	-	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3. ON resistance test circuit and graphs

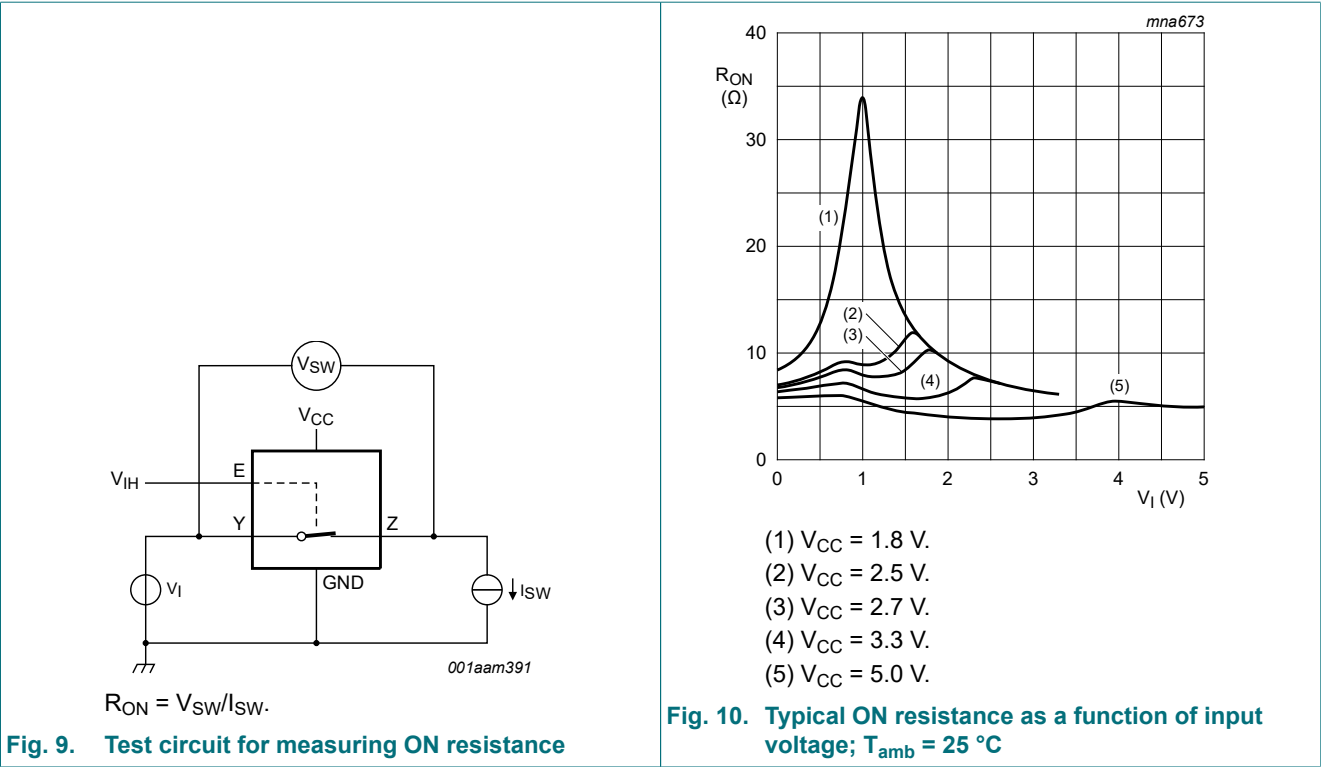


Fig. 9. Test circuit for measuring ON resistance

Fig. 10. Typical ON resistance as a function of input voltage; T_{amb} = 25 °C

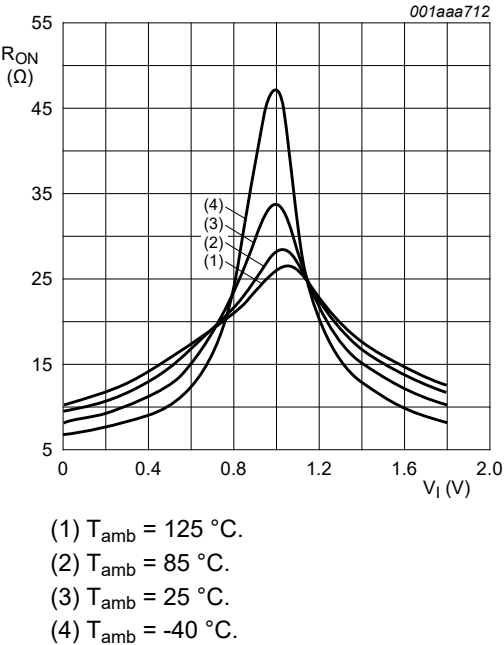


Fig. 11. ON resistance as a function of input voltage;
 $V_{CC} = 1.8$ V

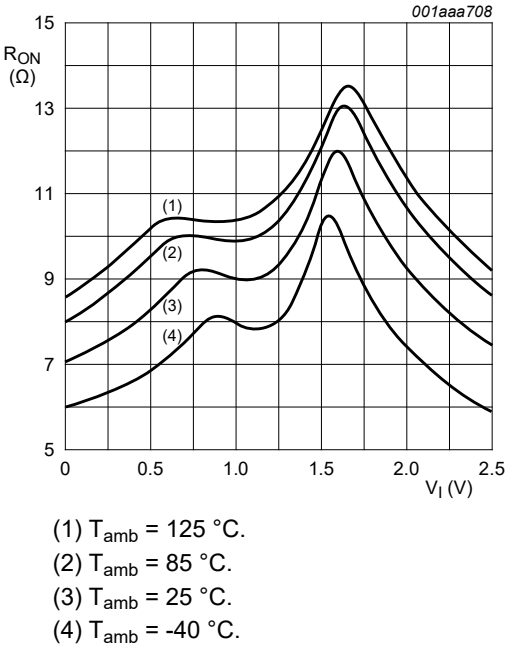


Fig. 12. ON resistance as a function of input voltage;
 $V_{CC} = 2.5$ V

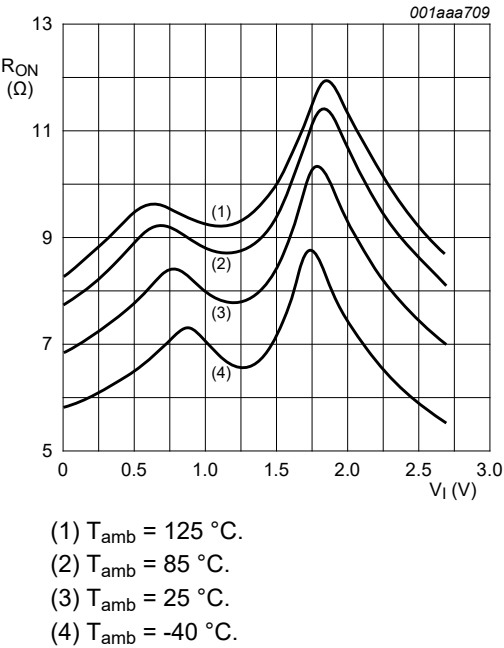


Fig. 13. ON resistance as a function of input voltage;
 $V_{CC} = 2.7$ V

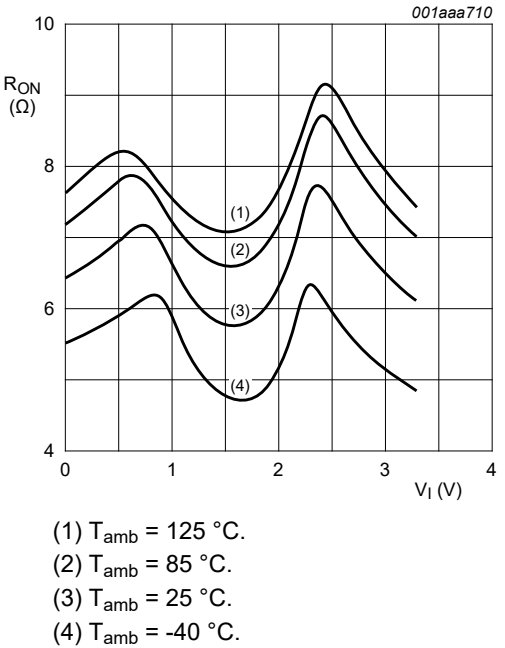


Fig. 14. ON resistance as a function of input voltage;
 $V_{CC} = 3.3$ V

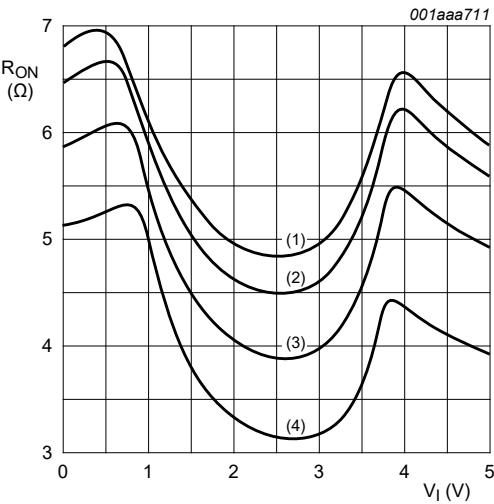


Fig. 15. ON resistance as a function of input voltage; $V_{CC} = 5.0\text{ V}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

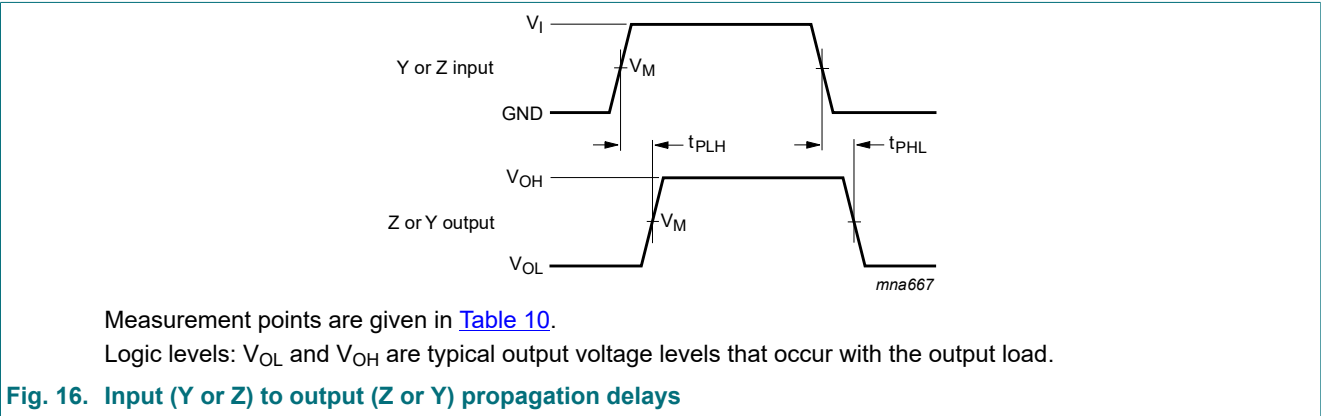
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 18.

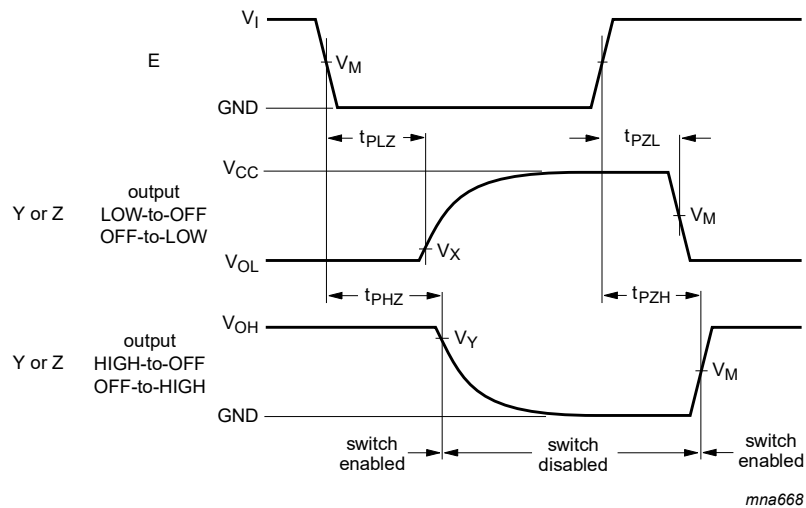
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	Y to Z or Z to Y; see Fig. 16 [2] [3]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	0.8	2.0	-	3.0	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	0.4	1.2	-	2.0	ns
		$V_{CC} = 2.7\text{ V}$	-	0.4	1.0	-	1.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	0.3	0.8	-	1.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	0.2	0.6	-	1.0	ns
t_{en}	enable time	E to Y or Z; see Fig. 17 [4]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.0	5.3	12	1.0	15.5	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.0	6.5	1.0	8.5	ns
		$V_{CC} = 2.7\text{ V}$	1.0	2.6	6.0	1.0	8.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.5	5.0	1.0	6.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	1.9	4.2	1.0	5.5	ns
t_{dis}	disable time	E to Y or Z; see Fig. 17 [5]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.0	4.2	10	1.0	13	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.4	6.9	1.0	9.0	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.6	7.5	1.0	9.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.4	6.5	1.0	8.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.5	5.0	1.0	6.5	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 10 MHz; V _I = GND to V _{CC} [6]						
		V _{CC} = 2.5 V	-	9.8	-	-	-	pF
		V _{CC} = 3.3 V	-	12.0	-	-	-	pF
		V _{CC} = 5.0 V	-	17.3	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).
- [4] t_{en} is the same as t_{PZH} and t_{PZL}.
- [5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
C_{S(ON)} = maximum ON-state switch capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
Σ{(C_L + C_{S(ON)}) × V_{CC}² × f_o} = sum of the outputs.

11.1. Waveforms and test circuit





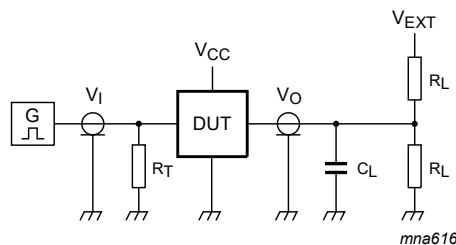
Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 17. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 11](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

V_{EXT} = External voltage for measuring switching times.

Fig. 18. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{CC}	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2V _{CC}
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2V _{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2V _{CC}

11.2. Additional dynamic characteristics

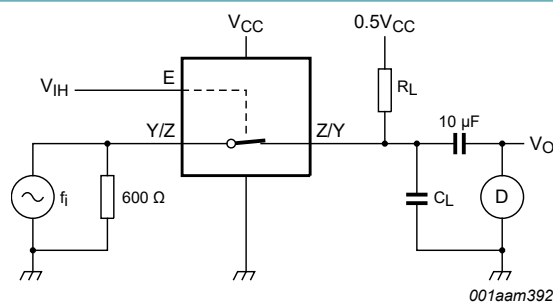
Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	R _L = 10 kΩ; C _L = 50 pF; f _i = 1 kHz; see Fig. 19				
		V _{CC} = 1.65 V	-	0.032	-	%
		V _{CC} = 2.3 V	-	0.008	-	%
		V _{CC} = 3.0 V	-	0.006	-	%
		V _{CC} = 4.5 V	-	0.001	-	%
		R _L = 10 kΩ; C _L = 50 pF; f _i = 10 kHz; see Fig. 19				
		V _{CC} = 1.65 V	-	0.068	-	%
		V _{CC} = 2.3 V	-	0.009	-	%
		V _{CC} = 3.0 V	-	0.008	-	%
		V _{CC} = 4.5 V	-	0.006	-	%
f _(-3dB)	-3 dB frequency response	R _L = 600 Ω; C _L = 50 pF; see Fig. 20				
		V _{CC} = 1.65 V	-	135	-	MHz
		V _{CC} = 2.3 V	-	145	-	MHz
		V _{CC} = 3.0 V	-	150	-	MHz
		V _{CC} = 4.5 V	-	155	-	MHz
		R _L = 50 Ω; C _L = 5 pF; see Fig. 20				
		V _{CC} = 1.65 V	-	> 500	-	MHz
		V _{CC} = 2.3 V	-	> 500	-	MHz
		V _{CC} = 3.0 V	-	> 500	-	MHz
		V _{CC} = 4.5 V	-	> 500	-	MHz
		R _L = 50 Ω; C _L = 10 pF; see Fig. 20				
		V _{CC} = 1.65 V	-	200	-	MHz
		V _{CC} = 2.3 V	-	350	-	MHz
		V _{CC} = 3.0 V	-	410	-	MHz
		V _{CC} = 4.5 V	-	440	-	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{iso}	isolation (OFF-state)	$R_L = 600\ \Omega$; $C_L = 50\ \text{pF}$; $f_i = 1\ \text{MHz}$; see Fig. 21				
		$V_{CC} = 1.65\ \text{V}$	-	-46	-	dB
		$V_{CC} = 2.3\ \text{V}$	-	-46	-	dB
		$V_{CC} = 3.0\ \text{V}$	-	-46	-	dB
		$V_{CC} = 4.5\ \text{V}$	-	-46	-	dB
		$R_L = 50\ \Omega$; $C_L = 5\ \text{pF}$; $f_i = 1\ \text{MHz}$; see Fig. 21				
		$V_{CC} = 1.65\ \text{V}$	-	-37	-	dB
		$V_{CC} = 2.3\ \text{V}$	-	-37	-	dB
		$V_{CC} = 3.0\ \text{V}$	-	-37	-	dB
		$V_{CC} = 4.5\ \text{V}$	-	-37	-	dB
V_{ct}	crosstalk voltage	between digital input and switch; $R_L = 600\ \Omega$; $C_L = 50\ \text{pF}$; $f_i = 1\ \text{MHz}$; $t_r = t_f = 2\ \text{ns}$; see Fig. 22				
		$V_{CC} = 1.65\ \text{V}$	-	69	-	mV
		$V_{CC} = 2.3\ \text{V}$	-	87	-	mV
		$V_{CC} = 3.0\ \text{V}$	-	156	-	mV
		$V_{CC} = 4.5\ \text{V}$	-	302	-	mV
Q_{inj}	charge injection	$C_L = 0.1\ \text{nF}$; $V_{gen} = 0\ \text{V}$; $R_{gen} = 0\ \Omega$; $f_i = 1\ \text{MHz}$; $R_L = 1\ \text{M}\Omega$; see Fig. 23				
		$V_{CC} = 1.8\ \text{V}$	-	3.3	-	pC
		$V_{CC} = 2.5\ \text{V}$	-	4.1	-	pC
		$V_{CC} = 3.3\ \text{V}$	-	5.0	-	pC
		$V_{CC} = 4.5\ \text{V}$	-	6.4	-	pC
		$V_{CC} = 5.5\ \text{V}$	-	7.5	-	pC

11.3. Test circuits



Test conditions:

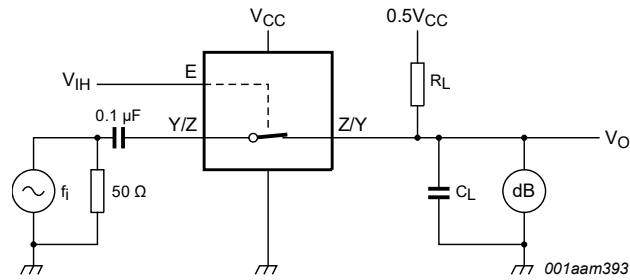
$V_{CC} = 1.65\ \text{V}$: $V_i = 1.4\ \text{V}$ (p-p).

$V_{CC} = 2.3\ \text{V}$: $V_i = 2\ \text{V}$ (p-p).

$V_{CC} = 3\ \text{V}$: $V_i = 2.5\ \text{V}$ (p-p).

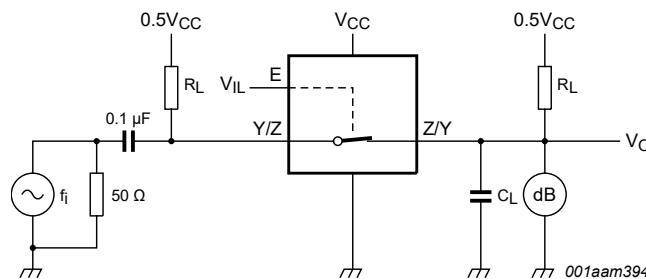
$V_{CC} = 4.5\ \text{V}$: $V_i = 4\ \text{V}$ (p-p).

Fig. 19. Test circuit for measuring total harmonic distortion



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 20. Test circuit for measuring the frequency response when switch is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 21. Test circuit for measuring isolation (OFF-state)

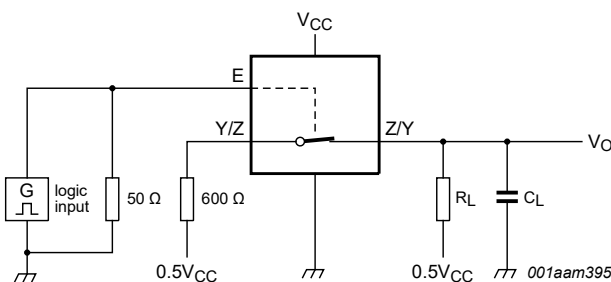
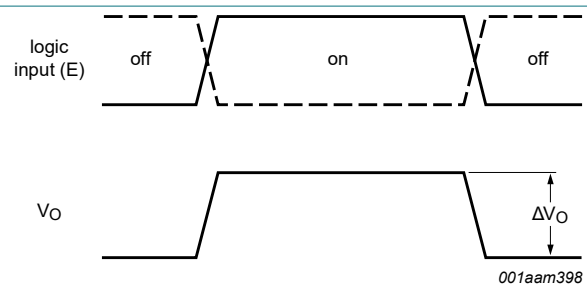
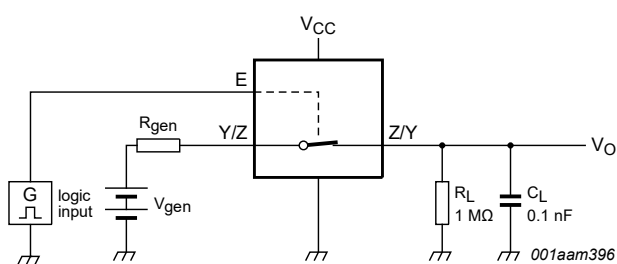


Fig. 22. Test circuit for measuring crosstalk between digital input and switch



$$Q_{inj} = \Delta V_O \times C_L.$$

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig. 23. Test circuit for measuring charge injection

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

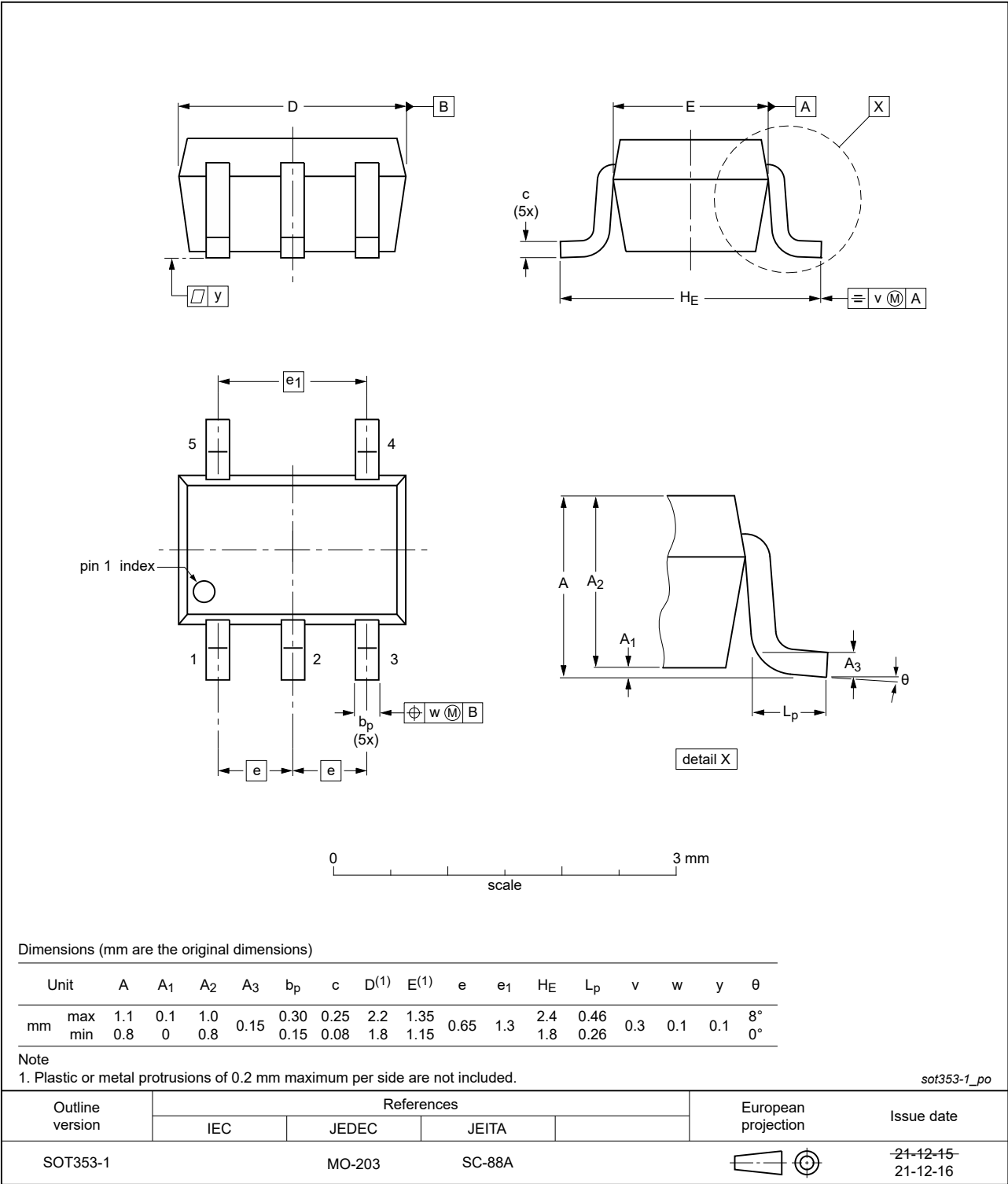


Fig. 24. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

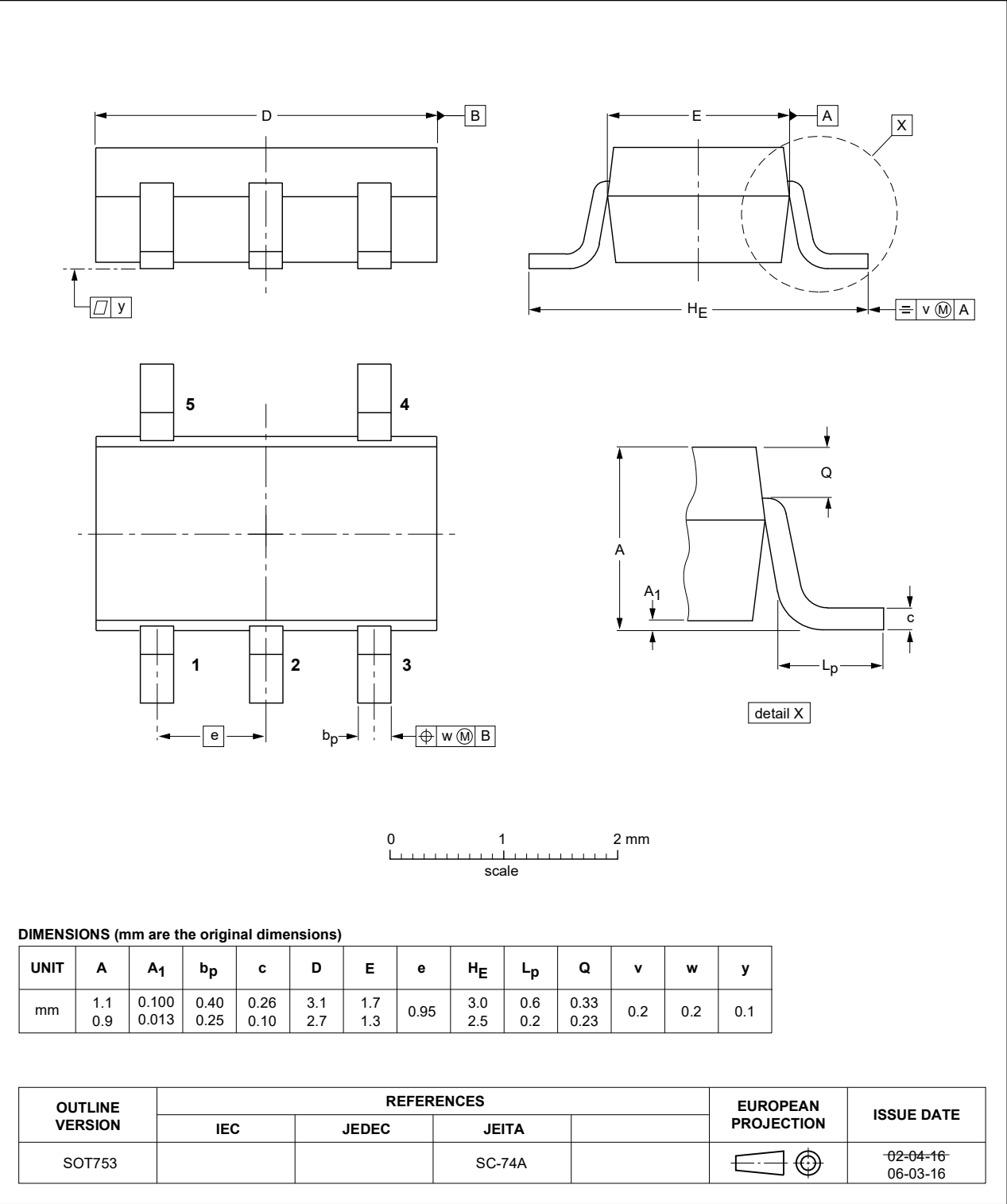


Fig. 25. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

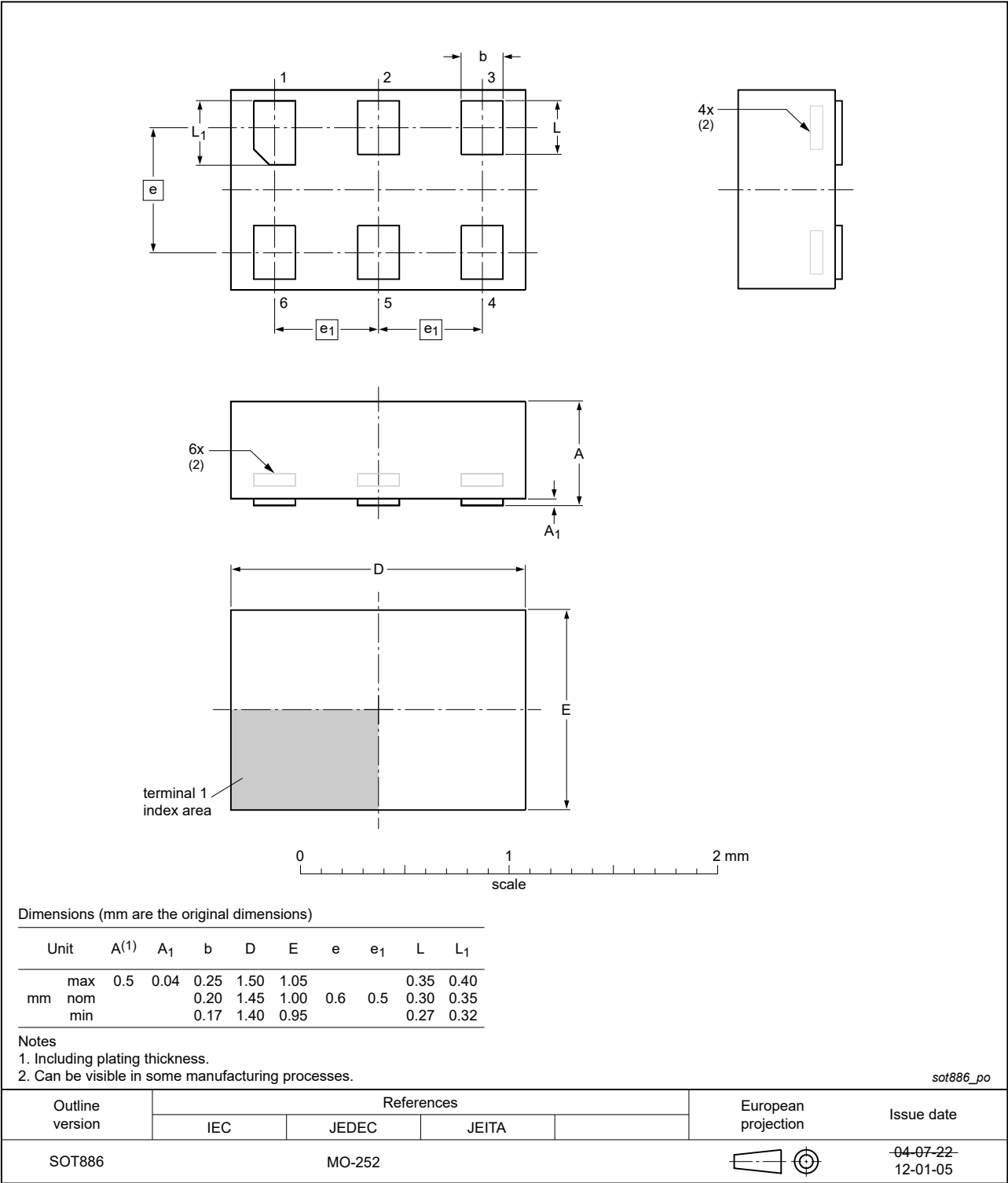


Fig. 26. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115

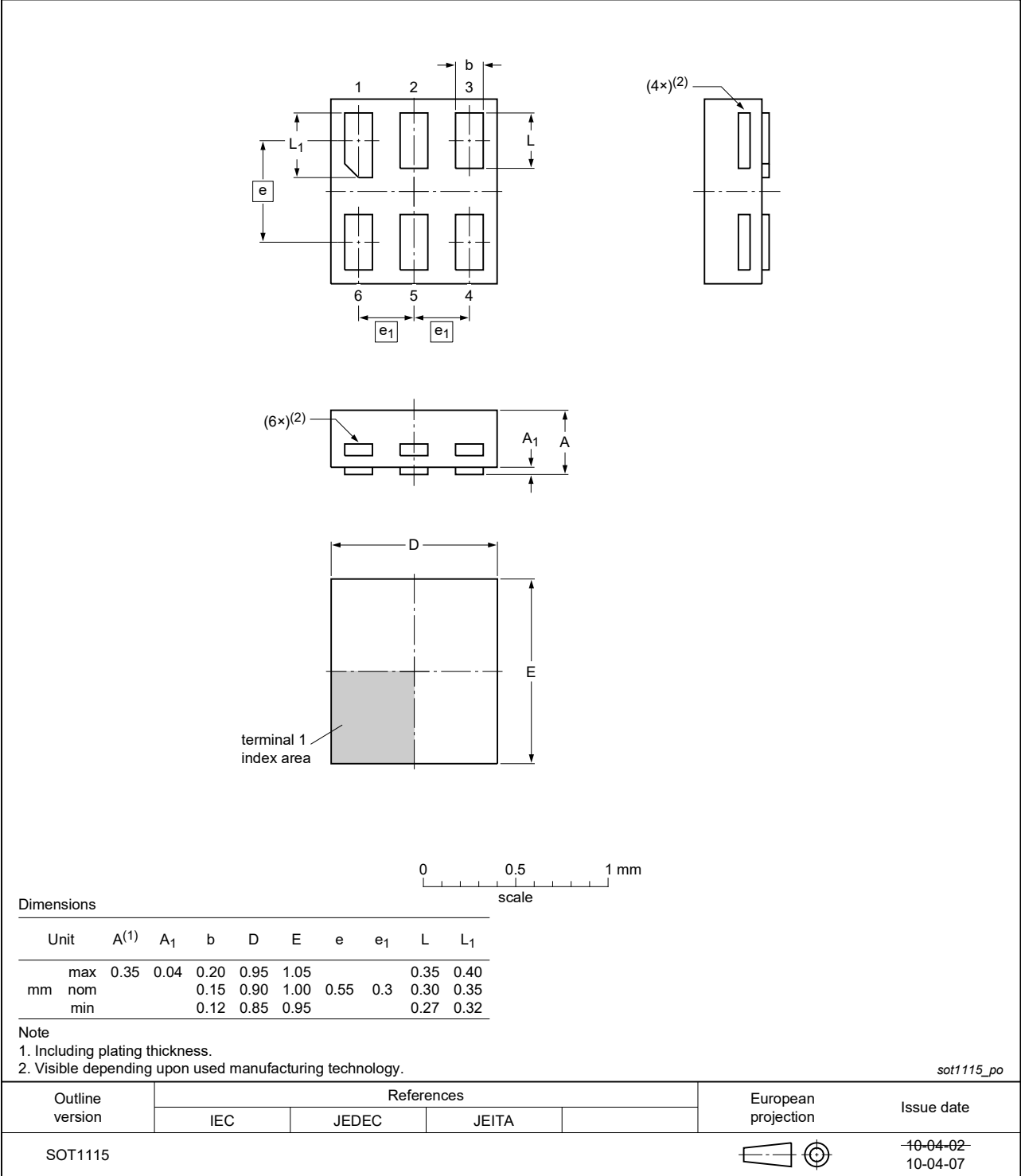
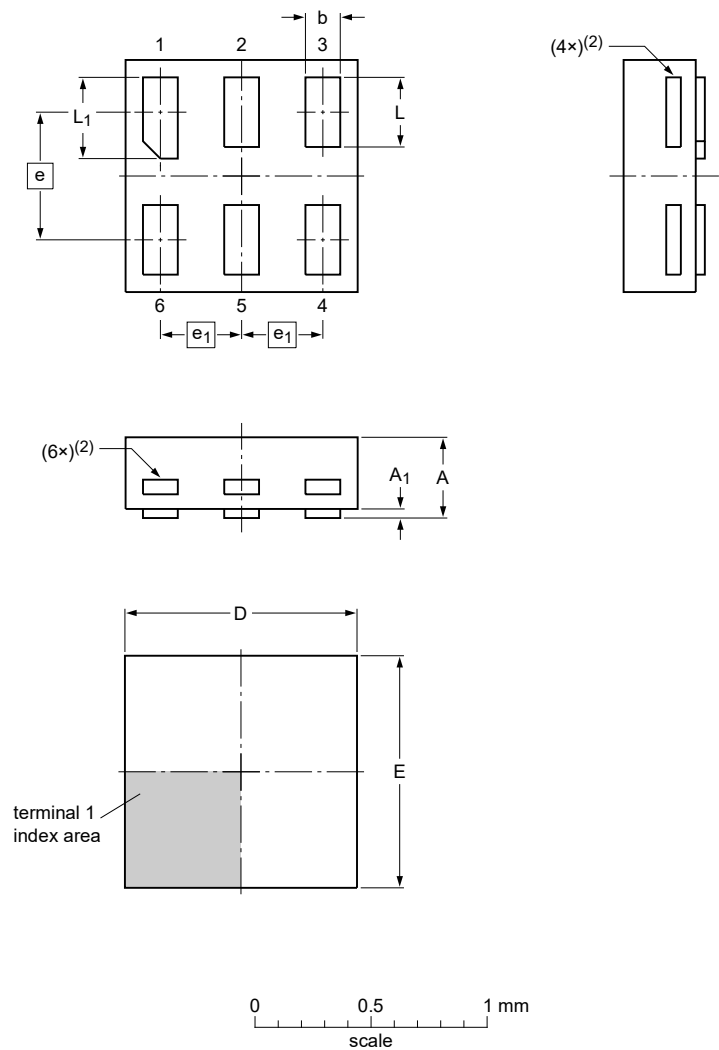


Fig. 27. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	1.05	1.05		0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.30	0.35
	min			0.12	0.95	0.95		0.27	0.32

Note

- 1. Including plating thickness.
- 2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						10-04-02 10-04-06

Fig. 28. Package outline SOT1202 (XSON6)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G66 v.12	20220112	Product data sheet	-	74LVC1G66 v.11
Modifications:	Fig. 24: Package outline drawing SOT353-1 (TSSOP5) has changed.			
74LVC1G66 v.11	20210608	Product data sheet	-	74LVC1G66 v.10
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74LVC1G66GF (SOT891 / XSON6) removed. Section 1 updated. Section 8: Derating values for P_{tot} total power dissipation updated.			
74LVC1G66 v.10	20161207	Product data sheet	-	74LVC1G66 v.9
Modifications:	Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC1G66 v.9	20150115	Product data sheet	-	74LVC1G66 v.8
Modifications:	SOT886 (XSON6) package outline drawing modified.			
74LVC1G66 v.8	20111202	Product data sheet	-	74LVC1G66 v.7
Modifications:	Legal pages updated.			
74LVC1G66 v.7	20100730	Product data sheet	-	74LVC1G66 v.6
74LVC1G66 v.6	20070827	Product data sheet	-	74LVC1G66 v.5
74LVC1G66 v.5	20070807	Product data sheet	-	74LVC1G66 v.4
74LVC1G66 v.4	20040413	Product specification	-	74LVC1G66 v.3
74LVC1G66 v.3	20021115	Product specification	-	74LVC1G66 v.2
74LVC1G66 v.2	20020529	Product specification	-	74LVC1G66 v.1
74LVC1G66 v.1	20011030	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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